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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 12/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,148	YOUNGS ET AL.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 1-68 are presented for examination.

Drawings

1. The drawings are objected to because Figure 2b does not properly identify the two lines "SHADOWA_SEL" and "SHADOWC_SEL" outputting from Test Controller 209b. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to because Figure 6 604 is incorrect. The examiner believes that "SET_S/NOP" should instead read "SET_X/NOP". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. New corrected drawings are required in this application because the drawings presented are hand drawn. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities: page 1 paragraph 2 refers to "core 101" twice in line 1, and also elsewhere in the specification. The examiner believes that this should recite "core 101a". Appropriate correction is required.

5. The disclosure is objected to because of the following informalities: page 6 paragraph 22 recites "multiplexer 214a". This multiplexer does not exist in the drawings. Appropriate correction is required.

6. The disclosure is objected to because of the following informalities: page 9 paragraph 32 line 2 cites "controller 209a", but the examiner believes this should recite "controller 209b". Appropriate correction is required.

7. The disclosure is objected to because of the following informalities: page 9 paragraph 33 line 4 reads "...and WE_C for port C", but the examiner believes this should read "...and WE_C 292 for port C". Appropriate correction is required.

8. The disclosure is objected to because of the following informalities: page 10 paragraph 34 line 5 reads "SHADOWC_Sel", but the examiner believes this should read "SHADOWC_Sel 276". Appropriate correction is required.

9. The disclosure is objected to because of the following informalities: page 10 paragraph 35 line 5 refers to "register 297" but the examiner believes this should read "register 246". Appropriate correction is required.

10. The disclosure is objected to because of the following informalities: page 13 paragraph 44 line 6 refers to "controller 209" but the examiner believes this should read "controller 209b". Appropriate correction is required.

11. The disclosure is objected to because of the following informalities: page 15 paragraph 50 line 4 refers to "register 245 for port A and register 246 for port B" but the examiner believes this should read "register 244 for port A and register 245 for port B" Appropriate correction is required.

12. The disclosure is objected to because of the following informalities: page 17 line 1 recites, "213 seen in Figure 2" but the examiner believes this should read "213 seen in Figure 2b". Appropriate correction is required.

13. The disclosure is objected to because of the following informalities: page 18 paragraph 59 line 5 refers to "combinations data" but the examiner believes this should read "combinations of data". Appropriate correction is required.

Claim Rejections - 35 USC § 112

14. Claim 28 recites the limitation "said last memory", "said last memory core", "said last controller" and "said upstream controller" in lines 1-3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15. Claims 1-3, 13-15, 17-19, 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ho-Ryong Kim, U.S. Patent No. 6122762, as being obvious.

As per Claim 1 and 13:

Kim teaches a memory apparatus comprising a controller (column 3 lines 36-40) coupled to a memory core through an interface circuit (see Fig. 4 of Kim), called the Debug Controller. Kim does not specifically state that the interface has an input that receives data from the system, with an output coupled to the memory. However, Kim performs the same functionality by combining the Debug Controller with a modified data

register (see column 6 lines 31-67). This arrangement of Debug Controller and data registers of Kim, couples system data to the memory core input as is claimed by the applicant. One with ordinary skill in the art at the time of the invention, motivated to provide a better method of interfacing a memory device in an embedded memory (as suggested in column 3 lines 8-54), would combine a multiplexer with the interface circuit as in Kim (Fig. 6). And one with ordinary skill in the art at the time of the invention would recognize that the Kim approach is the same as is claimed by the applicant, therefore Claims 1 and 13 are rejected.

As per Claim 2:

This claim, dependent on Claim 1, limits the controller to having a command input. Kim teaches this in Fig. 4. The Instruction Register 210 is under control of the TAP Controller, which is a widely used arrangement, and is well known in the art. Therefore, since Kim specifically teaches it, Claim 2 is rejected.

As per Claim 3:

This claim is dependent on Claim 2, limiting the instructions to a test command. Kim, in column 5 lines 33-39, fully teaches this, and therefore Claim 3 is rejected.

As per Claims 14 and 15:

These claims, dependent on Claim 13 above, specify a second input to the multiplexer to be selective of system or test data under control of a test enable signal. Kim, in Fig. 6 and column 6 lines 31-67 teaches this circuit, therefore Claims 14 and 15 are rejected.

As per Claims 17 & 18:

This claim is dependent on Claim 1, and specifies that the interface circuit (Debug Controller) couples test data to a register. Kim, in Figure 6 (Sin) teaches the loading of test data during debug mode into the latches (Figure 6 AC1...AC16) and the output coupled to a multiplexer (Figure 6 BI1...BI16), therefore, Claims 17 & 18 are rejected.

As per Claim 19:

Dependent on Claim 18 above, multiplexer (Kim, Figure 6 BI1...BI16) is selected to an output (Kim, Figure 6 BF1...BF16) if selected as a target port. But this claim does not disclose a multi-port memory which would require a target port. The examiner does not see a "target port" as being germain to the claim, and so the teachings of Kim are fully disclosed based upon the Kim references stated here, and Claim 19 is rejected.

As per Claim 21:

Dependent on Claim 1, specifies an output for sending a command to a downstream controller in a daisy chain, Kim in column 5 lines 39-65 teaches this, and so Claim 21 is rejected.

As per Claims 22-24:

These claims, dependent on Claim 1, specify the memory core to be RAM, ROM, and CAM. The patent issued to Kim, in column 3 lines 9-13, and in the Abstract, disclose the subject to be a "integrated circuit memory", and one with ordinary skill in the art at the time of the invention would interpret this to encompass all three claimed types of memory, therefore Claims 22-24 are rejected.

16. Claims 4-12, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ho-Ryong Kim, U.S. Patent No. 6122762, and in view of "Considerations for implementing IEEE 1149.1 on system-on-a-chip integrated circuits", Steven F. Oakland, Test Conference, 2000. Proceedings International , 3-5 Oct. 2000, pp 628 -637.

As per Claim 4:

This claim is dependent on Claim 3 and further defines the test command to being a PRELOAD WRITE. Although Kim does not name the command, the recital of column 7 lines 22-67 and column 8 lines 1-4 (Kim) describes a process of setting address data in the address latches (see Fig. 7) in a similar manner in light of the specification for the subject command. And Oakland, on page 629, column 1 paragraphs 7 and 8, teaches that tools exist to take advantage of IEEE 1149.1 in the development of processors with features that control operations on the chip such as START, RUN, RESET, among others. One with ordinary skill in the art at the time of the invention, motivated to provide a better method of interfacing a memory device in an embedded memory (as suggested in column 3 lines 8-54), would interface with the memory core using latches as in Kim, and provide instructions to accomplish this through the teaching of Oakland. Therefore, Claim 4 is rejected.

As per Claim 5:

This claim is dependent on Claim 3 and further defines the test command to being a PRELOAD READ. Although Kim does not name the command, the recital of column 6 lines 31-67 and column 7 lines 1-22 (Kim) describes a process of setting data in the data latches (see Fig. 6) in a similar manner in light of the specification for the

subject command. And Oakland, on page 629, column 1 paragraphs 7 and 8, teaches that tools exist to take advantage of IEEE 1149.1 in the development of processors with features that control operations on the chip such as START, RUN, RESET, among others. One with ordinary skill in the art at the time of the invention, motivated to provide a better method of interfacing a memory device in an embedded memory (as suggested in Kim, column 3 lines 8-54), would interface with the memory core using latches as in Kim, and provide instructions to accomplish this through the teaching of Oakland. Therefore, Claim 5 is rejected.

As per Claims 6-9:

All of these subject claims, with a dependency on Claim 3 above, limit the test commands further to READ and WRITE commands, either full or partial words. Oakland, on page 629, column 1 paragraphs 7 and 8, teaches that tools exist to take advantage of IEEE 1149.1 in the development of processors with features that control operations on the chip such as START, RUN, RESET, among others. Using the tools available, the claimed commands would be encompassed in the teachings of Oakland as "typical processor control features" (page 629 paragraph 7). Therefore, as per Oakland's suggestion to build any command required, one would combine these teachings with Kim to apply and access data as is being claimed by the applicant. Therefore, Claims 6-9 are rejected.

As per Claims 10-12:

The claims are dependent on Claim 2, and the command input further relates to setting a device configuration wherein test commands are either ignored or executed.

Oakland, in pages 629 column 2 and 630 column 1 completely teaches this limitation. Therefore, Claims 10-12 are rejected.

17. Claims 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ho-Ryong Kim, U.S. Patent No. 6122762, and in view of "A 5 GB/s 9-Port Application Specific SRAM with Built-in Self Test", Wood et al., 1995 International Workshop on Mermory Technology, Design and Testing, 1995, 7-8 Aug 1995, pp 68-73. The claims, dependent on Claim 13 and 17 above disclose a multi-port memory. Wood, in an analogous art and using the same multiplexing scheme (see Figure 4 of Wood), broadly teaches such an arrangement in a 9-port memory, in relation to a TAP controlled BIST architecture. One with ordinary skill in the art at the time of the invention, motivated to provide a better method of interfacing a memory device in an embedded memory (as suggested in Kim, column 3 lines 8-54), would combine a multiplexer with the interface circuit as in Kim (Fig. 6) with the teachings of Wood as applied to multi-port memories. Therefore Claims 16 and 20 are rejected.

18. Claims 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimoto et al., U.S. Patent No. 6404684, in view of D'Sousa et al., U.S. Patent No. 5254942, and further in view of "Considerations for implementing IEEE 1149.1 on system-on-a-chip integrated circuits", Steven F. Oakland, Test Conference, 2000. Proceedings International , 3-5 Oct. 2000, pp 628 -637.

As per Claim 25:

Arimoto et al. recites a memory unit having a controller (FIG. 1 TIC, and column 7 lines 13-22) which is coupled to a memory core (FIG. 1 TIC, and column 8 lines 22-

39). However, Arimoto et al. does not specify a test unit connection as claimed by the applicant. However, in an analogous art, D'Sousa et al., in the Abstract, suggests using a "PC or workstation" to control testing, and connecting the same to the Test Access Port terminals of the controller. Neither reference above suggests that there be two or more memory units connected in line. However, both of the above references are IEEE 1149.1 enabled circuits, and Oakland teaches daisy-chaining several IEEE 1149.1 logic units (page 630 column 2), which could contain memory cores (page 629, column 1, last two paragraphs) in the exact manner as claimed by the applicant. In view of connecting a test unit, D'Sousa et al., in column 3 lines 32-45 exemplifies the advantages of providing a PC as the test unit, Oakland provides reasons for daisy chaining units together (page 637 column 1). One with ordinary skill in the art at the time of the invention, motivated as suggested by D'Sousa et al. and Oakland, would combine the teachings above, and therefore Claim 25 is rejected.

As per Claim 26:

Oakland, in Figure 2 of page 629 teaches this arrangement, and so Claim 26 is rejected.

As per Claim 27:

D'Sousa et al., in column 3 lines 33-45, teaches collecting response data in the PC/Test Unit using the IEEE 1149.1 TAP. One with ordinary skill in the art at the time of the invention, motivated to collect response data as suggested above in D'Souza et al., would connect the TDO output of the last controller to the input of the PC/Test Unit. Therefore, Claim 27 is rejected.

As per Claim 28:

Dependent on Claim 25, limits the apparatus to a two-memory core arrangement, with two controllers. Oakland, on page 629 and in Figure 2 exemplifies the attaching in a daisy-chain mode, several units together. This claim's specification falls within the scope of the teachings of Oakland, and therefore Claim 28 is rejected.

19. Claims 29-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimoto et al., U.S. Patent No. 6404684, in view of D'Sousa et al., U.S. Patent No. 5254942, in view of "Considerations for implementing IEEE 1149.1 on system-on-a-chip integrated circuits", Steven F. Oakland, Test Conference, 2000. Proceedings International , 3-5 Oct. 2000, pp 628 –637, and further in view of Ho-Ryong Kim, U.S. Patent No. 6122762.

As per Claim 29:

This claim, dependent on Claim 25, limits the controller to having a command input. Kim teaches this in Fig. 4. The Instruction Register 210 is under control of the TAP Controller, which is a widely used arrangement, and is well known in the art. Therefore, since Kim specifically teaches it, Claim 2 is rejected.

As per Claim 30:

This claim is dependent on Claim 25, limiting the instruction to a test command. Kim, in column 5 lines 33-39, fully teaches this, and therefore Claim 30 is rejected.

As per Claim 31:

This claim is dependent on Claim 30 and further defines the test command to being a PRELOAD WRITE. Although Kim does not name the command, the recital of

column 7 lines 22-67 and column 8 lines 1-4 (Kim) describes a process of setting address data in the address latches (see Fig. 7) in a similar manner in light of the specification for the subject command. And Oakland, on page 629, column 1 paragraphs 7 and 8, teaches that tools exist to take advantage of IEEE 1149.1 in the development of processors with features that control operations on the chip such as START, RUN, RESET, among others. One with ordinary skill in the art at the time of the invention, motivated to provide a better method of interfacing a memory device in an embedded memory (as suggested in column 3 lines 8-54), would interface with the memory core using latches as in Kim, and provide instructions to accomplish this through the teaching of Oakland. Therefore, Claim 31 is rejected.

As per Claim 32:

This claim is dependent on Claim 30 and further defines the test command to being a PRELOAD READ. Although Kim does not name the command, the recital of column 6 lines 31-67 and column 7 lines 1-22 (Kim) describes a process of setting data in the data latches (see Fig. 6) in a similar manner in light of the specification for the subject command. And Oakland, on page 629, column 1 paragraphs 7 and 8, teaches that tools exist to take advantage of IEEE 1149.1 in the development of processors with features that control operations on the chip such as START, RUN, RESET, among others. One with ordinary skill in the art at the time of the invention, motivated to provide a better method of interfacing a memory device in an embedded memory (as suggested in Kim, column 3 lines 8-54), would interface with the memory core using latches as in

Kim, and provide instructions to accomplish this through the teaching of Oakland. Therefore, Claim 32 is rejected.

As per Claims 33-36:

All of these subject claims, with a dependency on Claim 30 above, limit the test commands further to READ and WRITE commands, either full or partial words. Oakland, on page 629, column 1 paragraphs 7 and 8, teaches that tools exist to take advantage of IEEE 1149.1 in the development of processors with features that control operations on the chip such as START, RUN, RESET, among others. Using the tools available, the claimed commands would be encompassed in the teachings of Oakland as "typical processor control features" (page 629 paragraph 7). Therefore, as per Oakland's suggestion to build any command required, one would combine these teachings with Kim to apply and access data as is being claimed by the applicant. Therefore, Claims 33-36 are rejected.

As per Claims 37-40:

The claims are dependent on Claim 29, and the command input further relates to setting a device configuration wherein test commands are either ignored or executed. Oakland, in pages 629 column 2 and 630 column 1 completely teaches this limitation. Therefore, Claims 37-40 are rejected.

20. Claims 41, 42, and 47-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimoto et al., U.S. Patent No. 6404684, in view of "Considerations for implementing IEEE 1149.1 on system-on-a-chip integrated circuits", Steven F.

Oakland, Test Conference, 2000. Proceedings International, 3-5 Oct. 2000, pp 628 – 637.

As per Claim 41:

A method of executing instructions on a memory core is taught by Arimoto et al. (column 3 lines 15-32) and the basis on whether the command applies to that memory core is taught by Oakland in pages 629 column 2 and 630 column 1. The Oakland reference teaches this limitation wherein test commands are either ignored or executed. One with ordinary skill in the art at the time of the invention, motivated to test several memory cores through a common interface (suggested by Oakland, page 630 column 1) would combine both references to achieve that goal. Therefore, Claim 41 is rejected.

As per Claim 42:

Claim 42, dependent on Claim 41, specifies that the controller (FIG. 14 TIC of Arimoto et al.) addresses memory with data supplied by the instruction. Arimoto et al. in column 3 lines 10-67 fully teaches this function. Therefore, Claim 42 is rejected.

As per Claims 47-50:

All of the subject claims, with a dependency on Claim 41 above, limit the test commands further to READ and WRITE commands, either full or partial words. Oakland, on page 629, column 1 paragraphs 7 and 8, teaches that tools exist to take advantage of IEEE 1149.1 in the development of processors with features that control operations on the chip such as START, RUN, RESET, among others. Using the tools available, the claimed commands would be encompassed in the teachings of Oakland as "typical processor control features" (page 629 paragraph 7). Therefore, as per

Oakland's suggestion to build any command required, one would combine these teachings with Kim to apply and access data as is being claimed by the applicant. Therefore, Claims 47-50 are rejected.

21. Claims 43-46 and 57-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimoto et al., U.S. Patent No. 6404684, in view of "Considerations for implementing IEEE 1149.1 on system-on-a-chip integrated circuits", Steven F. Oakland, Test Conference, 2000. Proceedings International, 3-5 Oct. 2000, pp 628 – 637, and further in view of "A 5 GB/s 9-Port Application Specific SRAM with Built-in Self Test", Wood et al., 1995 International Workshop on Memory Technology, Design and Testing, 1995, 7-8 Aug 1995, pp 68-73.

As per Claims 43 and 44:

These claims are dependent on Claim 41, and limit the memory core to being a multi-port memory, and the data to be written is applied to an input port. Claim 44 limits the test instruction to specifying the input data port. Wood et al. teaches this broadly in the recitation beginning on page 72 and ending on page 73. Included in Figure 4 is the means of this method, which illustrates how selection is accomplished. All of the requirements of this claim are encompassed by the references, and so Claims 43 and 44 are rejected.

As per Claim 45 and 46:

These claims are dependent on Claim 41, and limit the memory core to being a multi-port memory, and the data to be read out of the memory is applied to an output port, and to a controller output, under control of the test instruction. Wood et al. teaches

this broadly in the recitation beginning on page 72 and ending on page 73. Included in Figure 4 is the means of this method, which illustrates how selection is accomplished. All of the requirements of this claim are encompassed by the references, and so Claims 45 and 46 are rejected.

As per Claims 57 and 58:

These claims are dependent on Claim 55, and limit the memory core to being a multi-port memory, and the data to be written is applied to an input port. Claim 44 limits the test instruction to specifying the input data port. Wood et al. teaches this broadly in the recitation beginning on page 72 and ending on page 73. Included in Figure 4 is the means of this method, which illustrates how selection is accomplished. All of the requirements of this claim are encompassed by the references, and so Claims 57 and 58 are rejected.

As per Claim 59 and 60:

These claims are dependent on Claim 55, and limit the memory core to being a multi-port memory, and the data to be read out of the memory is applied to an output port, and to a controller output, under control of the test instruction. Wood et al. teaches this broadly in the recitation beginning on page 72 and ending on page 73. Included in Figure 4 is the means of this method, which illustrates how selection is accomplished. All of the requirements of this claim are encompassed by the references, and so Claims 59 and 60 are rejected.

22. Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimoto et al., U.S. Patent No. 6404684, in view of "Considerations for implementing IEEE

1149.1 on system-on-a-chip integrated circuits", Steven F. Oakland, Test Conference, 2000. Proceedings International , 3-5 Oct. 2000, pp 628 –637, and further in view of D'Souza et al., U.S. Patent No. 5254942. This claim is dependent on Claim 41 and limits the test command as being sent by the test unit. D'Souza et al., in the Abstract, and column 3 lines 33-49 specifically teaches this. Therefore Claim 51 is rejected.

23. Claims 52-56 and 61-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over D'Souza et al., U.S. Patent No. 5254942, in view of Arimoto et al., U.S. Patent No. 6404684, in view of "Considerations for implementing IEEE 1149.1 on system-on-a-chip integrated circuits", Steven F. Oakland, Test Conference, 2000. Proceedings International, 3-5 Oct. 2000, pp 628 –637.

As per Claim 52:

D'Souza et al. teaches a test unit part (Abstract), and a method of executing instructions on a memory core is taught by Arimoto et al. (column 3 lines 15-32) and the basis on whether the command applies to that memory core is taught by Oakland in pages 629 column 2 and 630 column 1. The Oakland reference teaches this limitation wherein test commands are either ignored or executed. One with ordinary skill in the art at the time of the invention, motivated to test several memory cores through a common interface (suggested by Oakland, page 630 column 1) would combine all references to achieve that goal. Therefore, Claim 52 is rejected.

As per Claims 53-55:

The claims are dependent on Claim 52, and the command input further relates to setting a device configuration wherein test commands are either ignored or executed.

Oakland, in pages 629 column 2 and 630 column 1 completely teaches this limitation. Therefore, Claims 53-55 are rejected.

As per Claim 56:

Claim 56, dependent on Claim 55, specifies that the controller (FIG. 14 TIC of Arimoto et al.) addresses memory with data supplied by the instruction. Arimoto et al. in column 3 lines 10-67 fully teaches this function. Therefore, Claim 56 is rejected.

As per Claims 61-64:

All of the subject claims, with a dependency on Claim 55 above, limit the test commands further to READ and WRITE commands, either full or partial words. Oakland, on page 629, column 1 paragraphs 7 and 8, teaches that tools exist to take advantage of IEEE 1149.1 in the development of processors with features that control operations on the chip such as START, RUN, RESET, among others. Using the tools available, the claimed commands would be encompassed in the teachings of Oakland as "typical processor control features" (page 629 paragraph 7). Therefore, as per Oakland's suggestion to build any command required, one would combine these teachings with Kim to apply and access data as is being claimed by the applicant. Therefore, Claims 61-64 are rejected.

As per Claims 65-68:

Oakland on page 629 column 1 teaches that tools are available to develop circuits which interface with the standard 1149.1 TAP controller which would manipulate the embedded units effectively. Among functions contemplated were memory core loading and unloading (next to last paragraph). All of the activities claimed by the

applicant fall within the scope of Oakland's teaching, therefore Claims 65-68 are rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on weekdays, 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-2394.

John P Trimmings
Examiner
Art Unit 2133

jpt

Gary J. Lamarre
for

Albert DeCady
Primary Examiner